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EXAMINER	
JUNTIMA, NITTAYA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,552	JOHNSTON, DAVID	
	Examiner	Art Unit	
	NITTAYA JUNTIMA	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14,15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-15,17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 4/8/2008.

2. **Claims 1-12, 14-15, and 17-19** are pending; claims 13 and 16 were canceled.

3. **Claims 1-9, 15, and 16-19** remain rejected under 35 U.S.C. 102(e).

4. **Claims 10-12, and 14** remain rejected under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-6, 15, 17, and 19** are rejected under 35 U.S.C. 102(e) as being anticipated by art of record, Valenci (US 2003/0185220 A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding **claim 1**, Valenci teaches an apparatus (network adapter 80, Fig. 1), comprising:

A configuration module (rules memory 100a, Fig. 3) to store configuration information including instructions to reconfigure one or more hardware elements (action rules used to reconfigure one or more hardware elements of the action module 160, Fig. 3 which

processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware). See paragraphs 32, 35-36, and 39 and steps 201, 203, 205, and 207 in Fig. 5A.

A hardware-based parsing module (rule-based parser 60b,Fig.3 and action module 160, Fig.3, collectively) to connect to said configuration module, said parsing module to receive a frame of information (a received packet on path 177, Fig. 3/step 195 in Fig 5A) and determine a frame format associated with said frame (identifying packet type in step 201, Fig. 5A), retrieve configuration information corresponding to said frame format and reconfigure a set of hardware elements to parse said frame based on the retrieved configuration information (parsing actions are retrieved and performed on the received packet based on the packet type by hardware components of the rule-based "hardware" parser 60b in Fig. 3, and the action module 160, Fig. 3 processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware as shown in steps 205 and 207 in Fig. 5A, see also paragraphs 27, 30, 35-36, 39-40).

Regarding **claim 2**, Valenci teaches that said parsing module outputs a field type for said frame (packet type of the received packet is identified by the rule-based parser 60b, Fig.3, see step 203 in Fig. 5A and paragraphs 35, 39-40).

Regarding **claim 3**, Valenci also teaches that said parsing module comprises a table driven non-deterministic push down finite automaton (since a table driven non-deterministic push down finite automaton is not defined, the claim is interpreted as the rule based parser 60b

using a parser table/TABLE 1 representing a state machine 180 to classify packet and split data from packet header, paragraphs 33 and 35).

Regarding **claim 4**, Valenci teaches that said configuration module (rules memory 100a, Fig. 3) comprises:

A state table module to store state information (TABLE 1/parser table contains state information, i.e., S_0, S_1, S_2…, paragraph 33).

A transition table module to store transition information (TABLE 1/parser table contains transition information, i.e., PRE and POST States, paragraphs 33 and 34).

Regarding **claim 5**, Valenci teaches a stack to connect to said parsing module (a software stack must be connected to rule-based parser 60B and action module 160 as a verifier to check whether the parsing was addressed correctly based on these partial rules 170 which are part of memory 100a in a case of any memory space limitations, see Fig. 3 and paragraph 38), and a mapping module to connect to said parsing module (a mapping module must be connected to map/associate the packet type with the parsed state, paragraph 39 and Fig. 5A, step 203).

Regarding **claim 6**, Valenci also teaches a delay line module (FIFO) to buffer said frame during said frame parsing (a FIFO used for "on-the-fly" parsing, paragraph 35).

Regarding **claim 15**, Valenci teaches a method (Fig. 5A) to perform frame parsing, comprising:

Receiving a frame (packet) of information (step 195, paragraph 39).

Determining a frame format (packet type) associated with said frame (step 201, paragraph 39).

Retrieving configuration information (action rules) from a configuration module (action rules memory 175, Fig.3) corresponding to said frame format, the configuration information including instructions to reconfigure one or more hardware elements (the action module 160 processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware, paragraphs 30, 32, 36, steps 203-207, Fig. 5A).

Reconfiguring a parsing module (action module 160, Fig.3) to parse said frame of information using said configuration information (the action module 160 processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware, Figs. 5A, steps 205,207, see also paragraphs 27, 30, 35-36, 39).

Parsing said frame for frame format information using said reconfigured parsing module (Fig. 5A, steps 205 or 207, e.g., breaking TCP packet into TCP data and TCP header, see also paragraphs 27, 35-39).

Regarding **claim 17**, Valenci teaches that said configuration information comprises state information from a state table and transition information from a transition table (action rules use the state machine 180,Fig.4 which is represented by parser table/TABLE 1 containing state information i.e., S_0, S_1, S_2…, and transition information, i.e., PRE and POST States, see claim 8, paragraphs 33-38).

Regarding **claim 19**, Valenci further teaches delaying said frame until said frame format information is parsed (the packet is not forwarded to the host system 30a,Fig. 2 until being processed by the action module 10, Fig.3, see the last five lines of paragraph 32).

7. **Claims 1-2, 7-9, 15, and 18** are rejected under 35 U.S.C. 102(e) as being anticipated by Sarkinen (US 6,904,057 B2).

Regarding **claim 1**, as shown in Fig. 3, Sarkinen teaches an apparatus, comprising:

A configuration module (element 320) to store configuration information including instructions (parsing instructions 322) to reconfigure one or more hardware elements (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

A hardware-based parsing module (elements 310 and 330 constitute a hardware-based parsing module) to connect to said configuration module, said parsing module to receive a frame of information (incoming frame 314) and determine a frame format associated with said frame (the preliminary multi-protocol frame classification 312), retrieve configuration information corresponding to said frame format (parsing instructions 322), and reconfigure a set of hardware elements to parse said frame based on the retrieved configuration information (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10,

lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, and Fig. 7, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

Regarding **claim 2**, Sarkinen teaches that said parsing module (elements 310 and 330,Fig.3 constitute a parsing module) outputs a field type for said frame (search results 322,Fig.3 represent information about the incoming frame 314, e.g, identification of the fields in the packet/the frame classification, col. 10, lines 49-50, 59-62 and col. 12, lines 61-64).

Regarding **claim 7**, Sarkinen also teaches that said parsing module (elements 310 and 330,Fig.3 constitute a parsing module) comprises a microcode sequencer (col. 11, lines 14-16).

Regarding **claim 8**, Sarkinen further teaches that said configuration module (element 320,Fig.3) comprises microcode memory (memory 430, Fig.4) to store mask data (bit mask, col. 11, lines 14-23, 44-59, col. 12, lines 36-38, 48-53), compare data (instructions for relative compare/fixed compare, col. 12, lines 36-38, 48-53), branch addresses (branch instructions, col. 12, lines 36-38, 48-60) and field types (field's predetermined conditions, col. 12, lines 48-60 and col. 13, lines 59-64).

Regarding **claim 9**, Sarkinen also teaches a delay line module (the dual port memory buffer 416 in Fig. 4) to buffer said frame during said frame parsing (col. 12, lines 24-26, 36-42, 64-col. 13, lines 1-3).

Regarding **claim 15**, Sarkinen teaches a method (Fig. 3) to perform frame parsing, comprising:

Receiving a frame of information (receiving incoming frame 314, col. 10, lines 39-42).

Determining a frame format associated with said frame (the preliminary multi-protocol frame classification 312 for frame 314 is produced, col. 10, lines 39-42).

Retrieving configuration information (parsing instructions 322, Fig.3) from a configuration module (a parsing instructions generator 320,Fig.3) corresponding to said frame format (col. 10, lines 42-45, see also step 712 in Fig. 7), the configuration information using instructions to reconfigure one or more hardware elements (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, and Fig. 7, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

Reconfiguring a parsing module to parse said frame of information using said configuration information (parsing instructions 322 are used to control a multi-stage parsing engine 330 for processing frame 314, col. 10, lines 42-48, 59-62, col. 11, lines 14-23).

Parsing said frame for frame format information using said reconfigured parsing module (a multi-stage parsing engine 330 parses frame 314 using parsing instructions 322, col. 10, lines 45-48, 59-62).

Regarding **claim 18**, Sarkinen further teaches that said configuration information (parsing instructions 322, Fig.3) comprises microcode information (microcode instruction set) from a microcode module (microcode module reads on means that generates microcode instruction set, col. 10, lines 59-62 and col. 11, lines 14-23).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 10 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over an art of record, Korpela (EP 0 852 448 A1) in view of Sarkinen (US 6,904,057 B2).

Regarding **claim 10**, Korpela teaches a system (Fig. 1), comprising:

At least one base station (radio access networks 20a, 20b, 20c, Fig. 1) to communication frames of information using a plurality of different frame formats (col. 4, lines 12-16, col. 8, lines 50-56)

A mobile station (mobile terminal 10, Fig. 1) to receive said frames of information, said mobile station comprising a receiver (RF circuit 12, digital signal processor device 13, and control device 15 constitute a receiver) to receive and process said frames (col. 4, lines 25-40, col. 8, lines 50-56).

However, Korpela does not teach that said receiver comprises reconfigurable hardware-based frame parser comprising a configuration module and a parsing module as claimed.

In an analogous art of multi-frame-format processing, Sarkinen teaches a network device 100 in Fig. 1 (equivalent to a receiver) that includes Frame/Medium Access Control 112 and a differentiated services routing and policing engine 120 in Fig. 1, collectively, for providing *multi-protocol*, multi-stage, real-time frame classification and generating search results using a preliminary multi-protocol frame classification and parsing instructions generated for incoming frames (col. 9, lines 58-67-col. 10, lines 3) comprising a classifier 300 in Fig. 3 (equivalent to a reconfigurable hardware-based frame parser) that comprises:

A configuration module (element 320) to store configuration information including instructions (parsing instructions 322) to reconfigure one or more hardware elements (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, and Fig. 7, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

A parsing module (elements 310 and 330 constitute a parsing module) to connect to said configuration module, said parsing module to receive a frame of information (incoming frame 314) and determine a frame format associated with said frame (the preliminary multi-protocol frame classification 312), retrieve configuration information corresponding to said frame format (parsing instructions 322), and reconfigure a set of hardware elements to parse said frame in

accordance with said different frame formats and the retrieved configuration information (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, and Fig. 7, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

Given the teaching of Sarkinen, it would have been obvious to one skilled in the art at the time the invention was made to modify the Korpela such that said receiver would comprise reconfigurable hardware-based frame parser comprising a configuration module and a parsing module as claimed. The suggestion/motivation to do so would have been to provide a parser that is programmable to build search words based on the preliminary multi-protocol frame classification and parsing instructions as suggested by Sarkinen (col. 10, lines 39-48 and col. 11, lines 15-16).

Regarding **claim 14**, Korpela does not teach a delay line module for buffering said frame during said frame parsing.

However, Sarkinen teaches a dual port memory buffer 416 in Fig. 4 for buffering a frame during frame parsing (equivalent to a delay line module). See col. 12, lines 24-26, 36-42, 64-col. 13, lines 1-3.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the teaching of Korpela to include a delay line module as claimed. The suggestion/motivation to do so would have been to have the frame written into the buffer and

read out from after frame processing is complete as taught by Sarkinen (col. 12, lines 64-col. 13, lines 3 and Fig. 4).

10. **Claims 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over an art of record, Korpela (EP 0 852 448 A1) in view of Sarkinen (US 6,904,057 B2), and further in view of Johnson (US 7,184,722 B1).

Regarding **claim 11**, although Korpela teaches the inherent MAC unit (the media access controller) for processing MAC layer (col. 6, lines 6-12), the combined teaching of Korpela and Sarkinen does not explicitly teach that the receiver comprises a power amplifier, an RF/IF converter to connect to said power amplifier, an IQ module to connect to said RF/RF converter, a baseband processor to connect to said IQ module and the media access controller.

However, Johnson teaches a wireless transmitter such as a mobile unit 18 in Fig. 2 for communicating to a plurality of base stations that includes a receiver (radio 60 working in a receiving direction as shown in Figs. 5A and 5B) comprising a power amplifier (amplifier 75,Fig.5A in the reception portion), an RF/IF converter (RF/IF converter 72,Fig.5A in the reception portion), an IQ module (I/Q modem 68,Fig. 5B in the reception portion), and a baseband processor (baseband processor PHY 66,Fig.5B in the reception portion) connecting to a MAC (MAC 64,Fig. 5B). See col. 8, lines 7-18, 41-col. 9, lines 1-42.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further modify the combined teaching of Korpela and Sarkinen such that the power amplifier, RF/IF converter, IQ module, and baseband processor would be connected to the

receiver and media access controller as claimed. The suggestion/motivation to do so would have been to enable the received wireless signal carrying data to be processed correctly.

Regarding **claim 12**, Korpela does not teach that the inherent MAC (see rejection of claim 10) comprises a reconfigurable hardware-based frame parser.

However, in an analogous art, Sarkinen teaches a Frame/Medium Access Control 112 and a differentiated services routing and policing engine 120 in Fig. 1, collectively, that comprises a classifier 300 in Fig. 3 which is a reconfigurable hardware-based frame parser as it provides *multi-protocol*, multi-stage, real-time frame classification and generates search results using a preliminary multi-protocol frame classification and parsing instructions generated for incoming frames (equivalent to a media access controller comprises a reconfigurable hard-ware-based frame parser). See col. 9, lines 58-60, 67-col. 10, lines 3, 27-48.

Given the teaching of Sarkinen, it would have been obvious to one skilled in the art at the time the invention was made to modify the combined teaching of Korpela and Johnson to further include a reconfigurable hardware-based frame parser as claimed. The suggestion/motivation to do so would have been to provide a parser that is programmable to build search words based on the preliminary multi-protocol frame classification and parsing instructions as suggested by Sarkinen (col. 10, lines 39-48 and col. 11, lines 15-16).

Response to Arguments

11. Applicant's arguments filed 4/28/2008 have been fully considered but they are not persuasive.

A. In the remarks on pages 7 and 8 regarding claims 1 and 15, Applicant argues that Sarkinen does not teach (i) the following language:

A configuration module to store configuration information including instructions to reconfigure one or more hardware elements and a hardware-based parsing module to connect to said configuration module…to…reconfigure a set of hardware elements to parse said frame based on the retrieved configuration information.

(ii) Sarkinen teaches a software based parsing engine that is loaded with different parsing instruction algorithms to manage different packet types which is in contrast to the claimed hardware based parsing module capable of reconfiguring a set of hardware elements based on retrieved configuration information.

In response, the Examiner respectfully disagrees. It is submitted that Sarkinen teaches (i) as follows:

A configuration module (element 320, Fig. 3) *to store configuration information including instructions* (parsing instructions 322) *to reconfigure one or more hardware elements* (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

A hardware-based parsing module (elements 310 and 330 constitute a parsing module) *to connect to said configuration module, ..to.. and reconfigure a set of hardware elements to parse said frame based on the retrieved configuration information* (the parsing engine 330 is programmable to build search words according to the microcode instructions, col. 10, lines 37-62, col. 11, lines 4-23, col. 12, lines 5-12, 24-col. 13, lines 14, and Fig. 7, therefore, hardware elements within 410 and 440 in Fig. 4 must be reconfigured in order to provide multi-stage parsing of the incoming frame 314 based on parser instruction set 436).

Regarding (ii), it is clear in Fig. 3 and 4 of Sarkinen that the combination of preliminary multi-protocol frame composition analyzer 310 and multi-state parsing engine 330 in Fig. 3 must be a hardware-based parsing module because:

- a preprocessor 410 in Fig. 4 that *is programmed* to classify the type of incoming frame (col. 12, lines 5-12);
- the parsing engine 330 as shown in Fig. 3/440 in Fig. 4 is part of *an apparatus* (col. 9, lines 23-25 and col. 10, lines 37-48 and col. 12, lines 5-7, 48-51), *parses the incoming frame* (col. 10, lines 59-62), *is programmable* to build search words and driven by a microcode controlled programmable sequencer implementation (col. 11, lines 14-16), and *executes a new instruction* each clock cycle (col. 13, lines 11-14);
- the process as shown in Fig. 7 implemented as computer program 262 *may be loaded into the classifier 210 in Fig. 2,* which contains elements 310 and 330 of Fig. 3, to cause the classifier 210 to perform the steps as taught by Sarkinen (col. 14, lines 9-19).

In other words, elements 310 and 330 of Sarkinen contain a combination of hardware elements that are reconfigurable based on retrieved instructions/microcode in order to parse a received frame according to its type.

Since there is no difference in structure or function between the teaching of Sarkinen and the claimed limitations, it is submitted that all claim limitations are met. Accordingly, the rejection is sustained.

B. In the remarks on pages 7 and 8 regarding claims 1 and 15, Applicant argues that Valenci does not teach (i) the language as recited in A above, and (ii) Valenci teaches a dynamic parser that is capable of using dynamically loaded parsing rules to change the behavior of the parser which is in contrast to the claimed hardware based parsing module capable of reconfiguring a set of hardware elements based on retrieved configuration information.

In response, the Examiner respectfully disagrees. It is submitted that Sarkinen teaches (i) as follows:

A configuration module (rules memory 100a, Fig. 3) *to store configuration information including instructions to reconfigure one or more hardware elements* (action rules used to reconfigure one or more hardware elements of the action module 160, Fig. 3 which processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware). See paragraphs 32, 35-36, and 39 and steps 201, 203, 205, and 207 in Fig. 5A.

A hardware-based parsing module (rule-based parser 60b,Fig.3 and action module 160, Fig.3, collectively) *to connect to said configuration module, ..to..reconfigure a set of hardware elements to parse said frame based on the retrieved configuration information* (parsing actions are retrieved and performed on the received packet based on the packet type by hardware components of the rule-based "hardware" parser 60b in Fig. 3, and the action module 160, Fig. 3 processes/splits the received packet according to loaded action rules, wherein the data splitting is performed by hardware as shown in steps 205 and 207 in Fig. 5A, see also paragraphs 27, 30, 35-36, 39-40).

Regarding (ii), it is clear that a rule-based parser 60b,Fig.3 and an action module 160, Fig.3, collectively, must be a hardware-based parsing module because:

- a rule-based parser 60b,Fig.3 is defined as *hardware* (paragraph 39);

- an action module 160, Fig.3 splits the data using *network hardware* based on action rules (paragraphs 35 and 36);

- in Fig. 8, the receive (Rx) portion, the receive dynamic parsers 60c, 60d may include one or more state machine, counter(s), and timer(s) (paragraph 52) and *packet parsing is done in network hardware* (paragraph 54).

In other words, a rule-based parser 60b,Fig.3 and an action module 160, Fig.3, of Valenci contain a combination of hardware elements that are reconfigurable based on the retrieved parsing/action rules in order to parse a received frame according to its type.

Since there is no difference in structure or function between the teaching of Valenci and the claimed limitations, it is submitted that all claim limitations are met. Accordingly, the rejection is sustained.

C. In the remarks on page 8 regarding claim 10, Applicant argues that Sarkinen fails to teach every limitation as recited in independent claims 1 and 15.

In response, in view of the explanation provided in section A above, it is submitted that Sarkinen teaches every limitation as claimed. In addition, the applicant fails to point out an error in the motivation. Therefore, the rejection is maintained.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NITTAYA JUNTIMA whose telephone number is (571)272-3120. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on 571-272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nittaya Juntima/
Examiner, Art Unit 2616
7/3/2008

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2616